**IN THE CLAIMS:**

Please substitute the following claims for the same-numbered claims in the application:

1. (Currently Amended) A field effect transistor (FET) comprising:

a source region;

a drain region;

a channel region disposed between the source and drain regions;

a bifurcated gate region positioned over said channel region; and

a gate oxide layer adjacent to said gate region, wherein said gate oxide layer comprises an alkali metal ion implanted at a dosage calculated based on threshold voltage test data provided by a post silicide electrical test conducted on said FET.

2. (Original) The transistor of claim 1, further comprising:

a substrate;

an isolation layer positioned over said substrate; and

at least one fin structure disposed between the source and drain regions;

wherein said source and drain regions are positioned over said isolation layer.

3. (Original) The transistor of claim 1, wherein said alkali metal ion comprises any of cesium and rubidium.

4. (Currently Amended) The transistor of claim 1, wherein said transistor ~~comprises~~ is one of a plurality of transistors comprised by a CMOS (complementary metal oxide semiconductor) device.

5. (Currently Amended) The transistor of claim 4, wherein said ~~CMOS device~~ plurality of transistors comprises any of a nFET ~~configuration~~ device and a pFET ~~configuration~~ device.

6. (Currently Amended) The transistor of claim [[5]] 1, ~~further comprising~~ wherein an ion implantation ~~levels for each of said nFET configuration and said pFET configuration of~~ level of said alkali metal ion is approximately $3 \times 10^{18}$ $cm^{-3}$.

7. (Original) The transistor of claim 1, wherein said gate region comprises silicide.

8. (Currently Amended) The transistor of claim 5, wherein said alkali metal ion adjusts nFET and pFET threshold voltages for the nFET and pFET ~~configurations~~ devices by an amount required to match desired off-currents for said nFET and pFET ~~configurations~~ devices.

9. (Currently Amended) A ~~(field effect transistor)~~ CMOS (complementary metal oxide semiconductor) device comprising:

raised ~~source/drain~~ source and drain regions;

a channel region disposed between said ~~source/drain~~ source and drain regions;

a gate region positioned over said channel region;

a silicon layer dividing said gate region; and

a gate oxide layer adjacent to said gate region, wherein said gate oxide layer comprises an alkali metal ion implanted at a dosage calculated based on threshold voltage test data provided by a post silicide electrical test conducted on said CMOS device.

10. (Currently Amended) The device of claim 9, further comprising:

a substrate;

an isolation layer positioned over said substrate; and

at least one fin structure disposed between ~~the~~ said source and drain regions;

wherein said ~~source/drain~~ source and drain regions are positioned over said isolation layer.

11. (Original) The device of claim 9, wherein said alkali metal ion comprises any of cesium and rubidium.

12. (Currently Amended) The device of claim 9, further comprising a plurality of FET (field effect transistor) devices, wherein said plurality of FET devices comprises any of a nFET ~~region~~ device and a pFET ~~region~~ device.

13. (Currently Amended) The device of claim ~~12~~ 9, ~~comprising~~ wherein an ion implantation ~~levels for each of said nFET region and pFET region of~~ level of said alkali metal ion is approximately $3 \times 10^{18}$ $cm^{-3}$.

14. (Currently Amended) The device of claim 9, further comprising spacers separating said gate region from said ~~source/drain~~ source and drain regions.

15. (Original) The device of claim 9, wherein said gate region comprises silicide.

16. (Currently Amended) The device of claim 12, wherein said alkali metal ion adjusts nFET and pFET threshold voltages for the nFET and pFET ~~regions~~ devices by an amount required to match desired off-currents for said nFET and pFET ~~regions~~ devices.

17-23. (Cancelled).

24. (New) The transistor of claim 1, further comprising spacers separating said gate region from said source and drain regions.

25. (New) The transistor of claim 1, wherein each of said source and drain regions comprise a semiconductor layer comprising said alkali metal ion.

26. (New) The transistor of claim 2, wherein said dosage of the alkali metal ion implantation is a function of a height of said fin structure divided by a thickness of said gate oxide multiplied by a calculated dosage level of said alkali metal ion implanted in a direction normal to said channel region.

27. (New) The transistor of claim 1, further comprising a silicide on said source and drain regions.

28. (New) The device of claim 9, wherein each of said source and drain regions comprise a semiconductor layer comprising said alkali metal ion.

29. (New) The device of claim 10, wherein said dosage of the alkali metal ion implantation is a function of a height of said fin structure divided by a thickness of said gate oxide multiplied by a calculated dosage level of said alkali metal ion implanted in a direction normal to said channel region.

30. (New) The device of claim 9, further comprising a silicide on said source and drain regions.